L Number	Hits	Search Text	DB	Time stamp
1	9002	functional adj2 unit$1	USPAT; US-PGPUB	2001/12/27 16:46
4	135652	power near3 control$5	USPAT; US-PGPUB	2001/12/27 16:46
7	26606	(insert$3 or add$3) with (program$3 or (instruction adj stream$1))	USPAT; US-PGPUB	2001/12/27 16:46
10	0	(functional adj2 unit$1) same (power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))	USPAT; US-PGPUB	2001/12/27 16:22
13	108	(functional adj2 unit$1) same (power near3 control$5)	USPAT; US-PGPUB	2001/12/27 16:22
16	9257	713/$.ccls.	USPAT; US-PGPUB	2001/12/27 16:22
22	5	((functional adj2 unit$1) same (power near3 control$5)) and ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))	USPAT; US-PGPUB	2001/12/27 16:23
19	22	713/$.ccls. and ((functional adj2 unit$1) same (power near3 control$5))	USPAT; US-PGPUB	2001/12/27 16:28
25	11332	(insert$3 or add$3) with (program$3 or (instruction adj stream$1))	EPO; JPO; DERWENT; IBM TDB	2001/12/27 16:46
30	136977	power near3 control$5	EPO; JPO; DERWENT; IBM TDB	2001/12/27 16:47
35	4412	functional adj2 unit$1	EPO; JPO; DERWENT; IBM TDB	2001/12/27 16:47
40	0	((insert$3 or add$3) with (program$3 or (instruction adj stream$1))) same (power near3 control$5) same (functional adj2 unit$1)	EPO; JPO; DERWENT; IBM TDB	2001/12/27 16:47
45	140	(power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))	USPAT; US-PGPUB	2001/12/27 17:01
48	0	((power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))) and ((functional adj2 unit$1) same (power near3 control$5))	USPAT; US-PGPUB	2001/12/27 17:02
51	12	((power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))) and 713/$.ccls.	USPAT; US-PGPUB	2001/12/27 17:06
54	202782	driver$1	USPAT; US-PGPUB	2001/12/27 17:06
57	10	driver$1 same ((power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1))))	USPAT; US-PGPUB	2001/12/27 17:10
60	1	(driver$1 same ((power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1))))) and 713/$.ccls.	USPAT; US-PGPUB	2001/12/27 17:10

Appl. No: 09/285,879

US-CL-CURRENT: 712/214,713/324

US-PAT-NO: 6219796
DOCUMENT-IDENTIFIER: US 6219796 B1
TITLE: Power reduction for processors by software control of functional units
DATE-ISSUED: April 17, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bartley; David Harold	Dallas	TX	N/A	N/A

US-CL-CURRENT: 713/320,712/214 ,713/324
ABSTRACT:
A method of optimizing a computer program for reduced power consumption by a processor (10) having functional units (11d, 11e) that are independently controllable by instructions. The processor's instruction set (FIG. 4) has instructions that may be directed to a particular functional unit (11d, 11e) so as to place that functional unit in a power-down state while not being used during a program segment.
9 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 4

BSPR:
One aspect of the invention is a method of optimizing a computer program for reduced power consumption. The method is used with programs written for a processor having distinct "functional units" to which instructions may be independently directed. The processor's instruction set is modified so as to provide special "power-down" instructions that may be directed to one or more functional units independently of other functional units. Then, for each functional unit, the computer program is scanned to locate segments of the program where that functional unit is not used. Based on the results of the scanning step, power-down instructions are **inserted into the program,** such that the functional unit uses less power while not in use. The method can be performed manually by an assembly language programmer or by a code optimization program.

BSPR:
A further advantage is that when a power-down instruction is used in accordance with the invention, the rest of the processor is fully operational. The program continues to execute as if the instructions were not there, because only functional units that are not used are affected. Thus, when **inserted** into a particular application **program,** the power-down instructions operate transparently to the programming in terms of both function and execution time.

DEPR:
Selective **Power Control of Functional Units** Referring again to FIG. 4, the instruction set of processor 10 is comprised of a number of instruction types, each of which may be executed by one or more **functional units**. These **functional units** are illustrated in FIG. 1, as the L, D, M, and S units of datapaths 11d and 11e.

DEPR:
Selective **Power Control of Other Functional Units**

DEPR:
Also, the same concepts can be applied to **power control of other functional units** within processor 10. For example, within CPU 11, subsets of the control registers 11f could be selected for power modification when not used. Other components suitable for power modification are specialized execution units such as floating point units and FFT units (not shown). Also, portions of memory 12 or memory 13 could similarly powered down. In general, the invention applies to the selective power-modification of any "**functional unit**" within processor 10, where the **functional unit** may either directly execute instructions or serve some peripheral function, and regardless of whether it is internal or external to the central processing unit 11.

DEPR:
One approach to implementing the method of FIG. 7 is for a **programmer** to manually scan the code and **insert** power-down instructions during the programming process. Alternatively, the method could be performed automatically by a compiler or ~~assembler~~. A compiler would have the overall function of operating on a higher-level language to create power-efficient machine code for processor 10. An assembler would operate on assembly code. /

CLPR:
3. The method of claim 1, further comprising the step of during **program** production prior to completion of said computer **program inserting** a power-up instruction in said computer **program**, wherein said power-up instruction directed to said at least one functional unit is operable to restore said at least one functional unit to a ready state.

CLPV:
wherein said **power-control** instruction is operable to cause said at least one **functional unit** to toggle between a full power ready state and a power-down state wherein said at least one **functional unit** consumes less power than in said ready state.

US-CL-CURRENT: 703/22

US-PAT-NO: 6125334
DOCUMENT-IDENTIFIER: US 6125334 A
TITLE: Module-configurable full-chip power profiler
DATE-ISSUED: September 26, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hurd; Linda L.	Sugarland	TX	N/A	N/A

US-CL-CURRENT: 702/60,703/22
ABSTRACT:

A method for determining the power consumption, resulting from execution of a block of code, of an integrated circuit that includes a processor module and one or more other circuit modules. The method involves the steps of, first, providing a set of average current values for each of said modules, for a predetermined plurality of sets of conditions based on predetermined sets of signal line states associated with said module, for each instruction in the instruction set of said processor module, said sets of conditions being selected for dominant power consumption effect on the module. For each module,
for each instruction in a block of code to be executed on said processor module, a set of signal line states is generated, associated with said module, for each processor cycle, in sequence. The generated set of signal line states
are then tested for said set of conditions. One of said average current values
is assigned for each condition so tested that is met. Finally, the running total of said average current values so met is accumulated for each such processor cycle. The average current values can be translated for different frequencies and supply voltages. Also, average current can be converted to average power consumption.
40 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

BSPR:
In U.S. Pat. No. 5,557,557, entitled "Processor Power Profiler," which issued
on Sep. 17, 1996, to Gene A. Frantz, et al., and which is commonly assigned, a method is presented for determining the energy consumption of a processor when executing a program. The method is embodied in a power profiler program, and initially selects the processor which will execute the program. It then creates a model of energy used by the processor as a function of a plurality of
instructions operable by the processor. The model is constructed based on measurements of the processor current taken under various controlled conditions. The program whose energy consumption is to be determined is then executed using the energy model to determine the energy consumption of the program on the processor. The energy model relates information regarding instruction opcodes, data values, processor environment, etc., to power data provided by a processor simulator or evaluator **program, and adds** the power data. The method groups certain instructions by common power considerations, and so partitioning of instructions is done in an early phase of the method, to
take advantage of this grouping.

DEPR:
Power consumption for control logic 204 is affected by the number of bits changing on the input signals, the number of bits changing on the control signals and the number of bits changing on the output signals. In addition, different modes of operation, such as receiving data versus processing data, have an affect on power consumption, as well. Pipeline phase differences also have an affect. Appendix 1 presents the role of the various control blocks and
functional units for different pipeline phases of the six instruction types.

US-CL-CURRENT: 713/310,713/321 ,713/324

US-PAT-NO: 6256743
DOCUMENT-IDENTIFIER: US 6256743 B1
TITLE: Selective power-down for high performance CPU/system
DATE-ISSUED: July 3, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Chong Ming	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 713/322,713/310 ,713/321 ,713/324
ABSTRACT:
A microelectronic device according to the present invention is made up of two or more functional units, which are all disposed on a single chip, or die. The present invention works on the strategy that all of the functional units on the die are not, and do not need to be operational at a given time in the execution of a computer program that is controlling the microelectronic device. The present invention on a very rapid basis (typically a half clock cycle), therefore, turns on and off the functional units of the microelectronic device in accordance with the requirements of the program being executed. This power down can be achieved by one of three techniques; turning off clock inputs to the functional units, interrupting the supply of power to the functional units, or deactivating input signals to the functional units. The operation of the present invention results in a very significant reduction in power consumption and corresponding heat dissipation by the microelectronic device as compared to the conventional approach of keeping all functional units operational all of the time.
8 Claims, 9 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 6

DEPR:
The present invention is a system and method for selectively **controlling the power provided to each of the functional units** of a microelectronic device so that the **functional units** can be turned on and off as needed by the execution of the computer program that is controlling the microelectronic device. The dynamic turning on and off of the **functional units** in accordance with the requirements of the program step(s) being executed causes a significant reduction in power (e.g., 10-30%) consumed by the **functional units,** which results in significant reduction in the heat dissipation requirements and a significant reduction in the power requirements of the microelectronic device. The present invention results in significant reduction in heat dissipation requirements and in power requirements for the microelectronic device, which means that heat sink requirements are reduced and battery discharge cycle length is extended, both of which are very desirable results. In addition, power bus line widths can be reduced. This leads to substantial area saving for VLSI chips.

DEPR:
Coupling/decoupling of a power supply bus is also envisioned. The addition of a power switch(es) connected between V.sub.DD and each **functional unit,** can be used to turn on and off the supply of **power to the functional units by controlling the power** switch (e.g., FET) using the above CKPWRON control

signal, or the like. In this power-down case, some DC power will be consumed through the power switch, but with the **functional unit**(s) disconnected, overall
conservation will result

CCOR:
713/322

CCXR:
713/310

CCXR:
713/321

CCXR:
713/324

US-CL-CURRENT: 712/214,**713/324**

US-PAT-NO: 6219796
DOCUMENT-IDENTIFIER: US 6219796 B1
TITLE: Power reduction for processors by software control of functional units
DATE-ISSUED: April 17, 2001
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bartley; David Harold	Dallas	TX	N/A	N/A

US-CL-CURRENT: **713/320**,712/214 ,**713/324**
ABSTRACT:
A method of optimizing a computer program for reduced power consumption by a processor (10) having functional units (11d, 11e) that are independently controllable by instructions. The processor's instruction set (FIG. 4) has instructions that may be directed to a particular functional unit (11d, 11e) so as to place that functional unit in a power-down state while not being used during a program segment.
9 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 4

DEPR:
Selective **Power Control of Functional Units** Referring again to FIG. 4, the instruction set of processor 10 is comprised of a number of instruction types, each of which may be executed by one or more **functional units**. These **functional units** are illustrated in FIG. 1, as the L, D, M, and S units of datapaths 11d and 11e.

DEPR:
Selective **Power Control of Other Functional Units**

DEPR:
Also, the same concepts can be applied to **power control of other functional units** within processor 10. For example, within CPU 11, subsets of the control registers 11f could be selected for power modification when not used. Other components suitable for power modification are specialized execution units such as floating point units and FFT units (not shown). Also, portions of memory 12 or memory 13 could similarly powered down. In general, the invention applies to the selective power-modification of any "**functional unit**" within processor 10, where the **functional unit** may either directly execute instructions or serve some peripheral function, and regardless of whether it is internal or external to the central processing unit 11.

CLPV:
wherein said **power-control** instruction is operable to cause said at least one **functional unit** to toggle between a full power ready state and a power-down state wherein said at least one **functional unit** consumes less power than in said ready state.

CCOR:

713/320

CCXR:
713/324

US-CL-CURRENT: 710/16,710/18 ,710/9 ,713/300 ,713/310 ,713/323 ,713/324

US-PAT-NO: 6115823
DOCUMENT-IDENTIFIER: US 6115823 A
TITLE: System and method for task performance based dynamic distributed power management in a computer system and design method therefor
DATE-ISSUED: September 5, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Velasco; Francisco	Los Gatos	CA	N/A	N/A
Phung; Xuyen N.	San Jose	CA	N/A	N/A
Mitchell; Phillip M.	San Jose	CA	N/A	N/A
Fung; Henry T.	San Jose	CA	N/A	N/A

US-CL-CURRENT: 713/322,710/16 ,710/18 ,710/9 ,713/300 ,713/310 ,713/323 ,713/324

ABSTRACT:
In a computer system having a device and a communications link for communicating with the device. A method for dynamically managing power consumption by the computer system comprises associating a particular device identifier with the device. Communications are monitored over the communications link to determine whether the communications include the particular device identifier. A clock input is withheld from the device when the communications do not include the particular device identifier. Clock input is provided to the device only when the communications include the particular device identifier. The clock input causes the device to transition from a non-operational power conservative state to an operational state wherein
the device consumes more power than in the non-operational state. A performance requirement is established for a task to be executed. Clock frequency is dynamically controlled according to the performance requirement established for the task being executed.
4 Claims, 49 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 44

BSPR:
In another aspect, the invention provides structure and method for a modular bus architectural (MBA) and fast modular bus architectural (FMBA) frames for System-on-a-Chip (SOC) designs including MBA/FMBA library modules that decrease
design time. In another aspect, the invention provides structure and method for adjusting bus clock speed in accordance with bus activity and task performance requirements so that further **control of power** consumption in the system is achieved without sacrificing performance. In one embodiment, the clock rate is adjusted in accordance with preassigned performance factors associated either with a **functional unit** or with a task type so that the task completes within a desired time without unnecessary power consumption. In another aspect, the FMBA/MBA is provided with a configurable interface that provides alternative single-edge and double-edge First-In-First-Out buffers. Among other advantages, these FIFO structures permit interconnection of MBA/FMBA modules at the core logic level, MBA/FMBA block level, and chip level so that systems are readily and reliable designed and implemented with minimum redesign.

CCOR:
713/322

CCXR:
713/300

CCXR:
713/310

CCXR:
713/323

CCXR:
713/324

US-CL-CURRENT: 713/320,713/321

US-PAT-NO: 6105139
DOCUMENT-IDENTIFIER: US 6105139 A
TITLE: Controller-based power management for low-power sequential circuits
DATE-ISSUED: August 15, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dey; Sujit	San Diego	CA	N/A	N/A
Raghunathan; Anand	Plainsboro	NJ	N/A	N/A
Jha; Niraj K.	Princeton	NJ	N/A	N/A

US-CL-CURRENT: 713/300,713/320 ,713/321
ABSTRACT:

A low-overhead **controller-based power** management technique that re-specifies control signals to reconfigure existing multiplexer networks and **functional units** to minimize unnecessary activity. Though the control signals in an RT-level implementation are fully specified, they can be re-specified under certain states/conditions when the data path components that they control need not be active. Another aspect of this invention is an algorithm to perform **power management through controller** re-specification, that consist of constructing an activity graph for each data path component, identifying conditions under which the component need not be active, and re-labeling the activity graph resulting in re-specification of the corresponding control expressions. The algorithm avoids the above negative effects of controller re-specification. Experimental results demonstrate that (i) controller re-specification allows us to perform efficient power management and obtain large **power savings for control**-flow intensive designs, which pose several challenges to conventional power management techniques, and (ii) it is important to consider the various potential negative effects while performing controller re-specification in order to obtain maximal power savings.

25 Claims, 43 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 20

ABPL:

A low-overhead **controller-based power** management technique that re-specifies control signals to reconfigure existing multiplexer networks and **functional units** to minimize unnecessary activity. Though the control signals in an RT-level implementation are fully specified, they can be re-specified under certain states/conditions when the data path components that they control need not be active. Another aspect of this invention is an algorithm to perform **power management through controller** re-specification, that consist of constructing an activity graph for each data path component, identifying conditions under which the component need not be active, and re-labeling the activity graph resulting in re-specification of the corresponding control expressions. The algorithm avoids the above negative effects of controller re-specification. Experimental results demonstrate that (i) controller re-specification allows us to perform efficient power management and obtain large **power savings for control**-flow intensive designs, which pose several challenges to conventional power management techniques, and (ii) it is important to consider the various potential negative effects while performing controller re-specification in order to obtain maximal power savings.

CCOR:

713/300

CCXR:
713/320

CCXR:
713/321

US-CL-CURRENT: 369/243,**713/300**

US-PAT-NO: 6094725
DOCUMENT-IDENTIFIER: US 6094725 A
TITLE: Magnetic disk apparatus
DATE-ISSUED: July 25, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hiyoshi; Yutaka	Yokohama	N/A	N/A	JPX
Tanaka; Hiroyuki	Kawasaki	N/A	N/A	JPX
Hakamatani; Takao	Kawasaki	N/A	N/A	JPX
Korikawa; Masayuki	Kawasaki	N/A	N/A	JPX
Tsurumi; Hiroshi	Kawasaki	N/A	N/A	JPX
Kudo; Tetsuro	Kawasaki	N/A	N/A	JPX
Ogawa; Yuiti	Yokohama	N/A	N/A	JPX

US-CL-CURRENT: **713/340**,369/243 ,**713/300**

ABSTRACT:
A magnetic disk apparatus includes at least two systems, each system having at least one power unit and at least one battery unit ancillary to the power unit. The disk apparatus also includes at least one common power unit having a pluralities of batteries attached thereto connected in common with the two systems. Patrol control means (PC) is operatively connected to a power control unit (0) of one system and a power control unit (1) of another system for giving a control signal during a battery monitoring operation and a priority order to the battery monitoring operation. The patrol control means monitors the function of the common batteries attached to the common power unit and, further, when the common batteries are incorporated in the magnetic disk apparatus, controls the simultaneous monitoring of the common batteries and the time of incorporation of the common batteries into the magnetic disk apparatus.
When one of the at least two systems is monitoring the common batteries, the power control unit of the one of the at least two system sends a master signal MAS to the patrol control means (PC) indicating that the one of the at least two systems is monitoring the common batteries, and the patrol control means sends an other-system patrol signal O-TST to the other of the at least two system indicating that the one of the two at least two system is monitoring the common batteries.
7 Claims, 56 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 62

BSPR:
The present invention further provides a magnetic disk control apparatus provided with at least a main power unit and a **functional unit** and performing the **control of the cut-off of the power,** wherein

DEPR:
FIG. 48 is a basic structural view of the conventional supply of **power and control** of cut-off. FIG. 49 is a flow chart of the **power cut-off control** system in the construction of FIG. 48. In FIG. 48, the magnetic disk control apparatus 720 is divided schematically into a main power unit 721 and a **functional unit** 722 for simplification of the explanation. Accordingly, the

power unit and the battery units are included in the main power unit 721 of the construction of FIG. 48. The rest of the construction is included in the **functional unit** 722. The first storage device 723 is a storage device for recording the history of occurrence of breakdowns such as stoppages of operation of the system. Note that IF is a **power control** interface between a higher apparatus 710 and the magnetic disk control apparatus 720, AC is AC power, and DC is DC power. Further, while explained in FIG. 49, RS is a power cut-off request signal sent from the power unit 721, and AS is a power cut-off authorization signal sent from the **functional unit** 722.

DEPR:
In FIG. 49, when the main power unit 721 receives an instruction for detection of a power failure or cut-off of power from the higher apparatus 710, such as a host computer, or by operation by an operator through a **power control** interface IF (S1), first, the main power unit 721 switches the power supply to the **functional unit** 722 from the power unit to the batteries (S2), then the main power unit 721 holds the battery output for a predetermined period (S3). That is, the construction enables the power of the system to be maintained for a predetermined period during a power failure by use of the back-up batteries. Next, the main power unit 721 sends out to the **functional unit** 722 a power cut-off request signal RS notifying it that it wishes to cut off the power.

DEPR:
In FIG. 47, in the same way as mentioned above, when the main power unit 721 receives an instruction for detection of a power failure or cut-off of power from a higher apparatus 710, such as a host computer, or by operation by an operator through a **power control** interface IF (S1), first, the main power unit 721 switches the power supply to the **functional unit** 722' from the power unit to the batteries (S2), then the main power unit 721 holds the battery output for a predetermined period (S3). That is, the construction enables the power of the system to be maintained for a predetermined period during a power failure by use of the back-up batteries. Next, the main power unit 721 sends out to the **functional unit** 722' a back-up signal BS notifying it that the batteries are being used due to a power failure and an automatic cut-off signal CS notifying it that it is desired to cut off the power automatically since the maximum discharge time of the batteries has been reached. The main power unit 721 next sends a power cut-off request signal RS to the **functional unit** 722'.

DEPR:
FIG. 52 is a basic structural view of a file control system, in particular, a structural view of key portions of a magnetic disk control apparatus. As mentioned earlier, the magnetic disk control apparatus is basically comprised of a main power unit 821 and a **functional unit** 822. The main power unit 821 is comprised of a power unit for converting AC voltage to DC voltage and supplying the same to the **functional unit** and battery units for providing back-up during power failures. Further, the **functional unit** 822 is mainly comprised of drive modules, not shown. In the figure, IF is a **power control** interface between the higher apparatus 810 and a power unit 821, RS is a power cut-off request signal sent out from the main power unit to the **functional unit** when the batteries

are
being used, and AS is a power cut-off authorization signal sent from the **functional unit** to the main power unit.

DEPR:
In the figure, C1 is a power-on signal from the **power control** interface 811, and C2 is a power-on signal from the power maintenance panel. C3 is an R/L signal from the R/L switch 812, and C4 is a power-on signal. The signals C3 and C4 are input to the **power control unit 813, while the power** input instruction signal C5 is sent to the power unit 821. As a result, the main power unit 821 can supply power to the **functional unit** 822. Note that D1 is a data bus for data sent out from the **power control** unit 13 to the panels 14 and 15.

CLPV:
at least a main power unit and a **functional unit** for performing a **control of a cut-off of power,**

CCOR:
713/340

CCXR:
713/300

US-PAT-NO: 6049882
DOCUMENT-IDENTIFIER: US 6049882 A
TITLE: Apparatus and method for reducing power consumption in a self-timed system
DATE-ISSUED: April 11, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Paver; Nigel C.	Manchester	N/A	N/A	GBX

US-CL-CURRENT: 713/322

ABSTRACT:
A power consumption control apparatus and method for an asynchronous system is provided that reduces power consumption by selecting one of a plurality of power consumption levels for the system. The power consumption levels can be determined based on work load requirements of the system and can be implemented
for the system or portions thereof using a single block of the system. The asynchronous system includes a plurality of intercoupled functional units and a
power control circuit coupled to a selected one of the plurality of functional units to determine at least one of a first and a second operating speed of a selected functional unit.
25 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

ABPL:
A power consumption control apparatus and method for an asynchronous system is provided that reduces power consumption by selecting one of a plurality of power consumption levels for the system. The power consumption levels can be determined based on work load requirements of the system and can be implemented
for the system or portions thereof using a single block of the system. The asynchronous system includes a plurality of intercoupled functional units and a
power control circuit coupled to a selected one of the plurality of functional units to determine at least one of a first and a second operating speed of a selected functional unit.

BSPR:
In order to achieve at least the above objects in a whole or in part, there is provided an asynchronous system according to the present invention that includes a plurality of functional units intercoupled to perform at least one task and a power control circuit coupled to a selected one of the plurality of functional units to determine at least one of a first and a second operating speed of the selected functional unit.

BSPR:
To further achieve the above objects in a whole or in part, there is provided a
data processing apparatus according to the present invention that includes a plurality of functional units, an asynchronous controller that decodes a current instruction to perform a corresponding instruction task using a group of the plurality of functional units, a power determination device, wherein the
data processing apparatus operates at one of a plurality of power levels selected by the power determination device and a communication device coupling

the functional units, the power determination device and the controller.

DEPR:
A third preferred embodiment according to the present invention uses the activation of particular functional units to control the power consumption. For example, a processor can be controlled to speed up or slow down based on a particular functional unit (e.g. a multiplier functional unit may require faster operation).

DEPR:
As described above, the preferred embodiments of the presentation control system power consumption using a variable delay in a functional unit to link cycle time to some measure of system load. However, the present invention is not intended to be limited to these embodiments. Various alternative indications of work load requirements such as application specific load indicators can be used to control the cycle time.

DEPR:
As well as controlling overall system performance, a fourth preferred embodiment according to the present invention controls power consumption of one
or more individual sub-circuits or sub-systems of an asynchronous system. In the fourth preferred embodiment, one variable delay unit is required per sub-system. The fourth preferred embodiment allows specific parts of the system to reduce power consumption relative to other parts of the system. In this manner, a first functional unit of a plurality of functional units in the system can selectively reduce its power consumption by executing at a lower priority than the remaining functional units.

CLPR:
4. The asynchronous system of claim 1, wherein the power control circuit selects a variable speed of operation for the selected functional unit.

CLPR:
8. The asynchronous system of claim 1, wherein the plurality of functional units is divided into a plurality of groups of functional units, and wherein the power control circuit comprises a plurality of power control units that each correspond to one of the group of functional units, and wherein each of the power control units sets a variable operating speed for the corresponding one of the groups of functional units using a designated functional unit in each of the groups of functional units.

CLPV:
a power control circuit coupled to a selected one of the plurality of functional units to determine at least one of a first and a second operating speed of the selected functional unit, wherein the operating speed of the selected functional unit determines an operating speed of the asynchronous system.

CLPV:
a communication device coupling the functional units, the power determination device and the controller, wherein power determination device modifies a cycle time without a clock signal.

CCOR:
713/322

US-CL-CURRENT: **713/324**

US-PAT-NO: 5996083
DOCUMENT-IDENTIFIER: US 5996083 A
TITLE: Microprocessor having software controllable power consumption
DATE-ISSUED: November 30, 1999
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
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US-CL-CURRENT: **713/322**,**713/324**

ABSTRACT:
A microprocessor is provided which includes a **power control** register for **controlling the rate of execution and therefore the power** consumption of individual **functional units**. The **power control** register includes a plurality of fields corresponding to the **functional units** for storing values that **control the power** consumption of each. The **power control** register fields can be set by software which has the much greater ability to look out into the future to determine whether the **functional units** will be required. The **functional units** are responsive to the corresponding **power control** register field to adjust their rate of execution responsive to the value stored therein. The rate of execution can be controlled in a number of different ways: dividing down the clock; removing power to the **functional unit**; disabling the sensor and/or buffer driver of one or more of the ports in a multi-ported RAM; removing data from the **functional unit**; and changing the data bus width responsive to the control register field. The microprocessor also includes a latency control register which assures that the **functional unit** is operational after the **functional unit** is placed from a low power state to a more fully operational state by changing the corresponding field in the **power control** register.
36 Claims, 11 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

ABPL:
A microprocessor is provided which includes a **power control** register for **controlling the rate of execution and therefore the power** consumption of individual **functional units**. The **power control** register includes a plurality of fields corresponding to the **functional units** for storing values that **control the power** consumption of each. The **power control** register fields can be set by software which has the much greater ability to look out into the future to determine whether the **functional units** will be required. The **functional units** are responsive to the corresponding **power control** register field to adjust their rate of execution responsive to the value stored therein. The rate of execution can be controlled in a number of different ways: dividing down the clock; removing power to the **functional unit**; disabling the sensor and/or buffer driver of one or more of the ports in a multi-ported RAM; removing data from the **functional unit**; and changing the data bus width responsive to the control register field. The microprocessor also includes a latency control register which assures that the **functional unit** is operational after the **functional unit** is placed from a low power state to a more fully operational

state by changing the corresponding field in the **power control** register.

BSPR:
A microprocessor is provided which includes improved power management facilities. The microprocessor includes a **power control** register that includes a plurality of fields for individually **controlling the power** consumption of the individual **functional units** within the microprocessor. The **power control** register fields can be set by software which has the much greater ability to look out into the future to determine whether the **functional units** will be required. This allows the microprocessor to shut down or adjust the execution rate of any one of the **functional units** when the software determines that the **functional unit** is not required by the currently executing software. This offloads the task of dynamically sensing and decoding instruction activity from the hardware to the software. In addition, software **control permits power** management capabilities not possible with hardware. For example, software can disable branch prediction hardware during execution of a certain block of code in order to save power. The software can also slow or shut down an external bus interface to main memory in the event a certain block of code is expected to fit entirely within an internal cache. Software possesses knowledge that is unavailable to hardware and can thus make more informed power management decisions that have the least impact on performance.

BSPR:
The **functional units** are responsive to the corresponding **power control** register field to adjust their rate of execution responsive to the value stored therein.
The rate of execution can be controlled in a number of different ways. First, the clock signal provided to the **functional unit** can be divided down responsive to the **power control** register field. This can be at an individual **functional unit** level such as where the **functional unit** is an I/O unit or at the global microprocessor level. Second, the rate of execution of the **functional unit** can be adjusted by removing power to the **functional unit** responsive to the **power control** register field. This can be accomplished by interposing a gating transistor between the **functional unit** and ground or, alternatively, between the **functional unit** and the supply voltage (V.sub.dd). In a third approach, used where the **functional unit** is a multiported random access memory (RAM), the sensor and/or buffer driver of one or more of the ports in the RAM are disabled responsive to the **power control** register field. By disabling one of the ports, the throughput or execution rate of the multiported RAM is reduced as is the power dissipated thereby. This is an example of a fourth and more general approach of removing data from the **functional unit** responsive to the control register field. This can be accomplished by disabling the tri-state buffers coupled between the data bus and the **functional unit**. In yet another approach, the **power control** register field can be used to switch between a 32 and 64 bit external interface to reduce the power of the I/O unit. This list of approaches is not exhaustive but illustrative of the power of the software approach to internal power management of a microprocessor.

BSPR:
In another aspect of the invention, the microprocessor includes a power latency register that stores a power latency value (PLV) in units of clock cycles. When the software issues an instruction to "wake up" (i.e., increase the activity and therefore power consumption level of) a **functional unit** by writing a value to the **power control** register, the unit will take some number of cycles before it becomes available. The PLV value represents the assumption by the software of how many cycles this wake up will take for the **functional unit** in question. This means the instruction stream is guaranteed to have no instructions that are relevant to the **functional unit** for PLV number of cycles after the unit's power latency register has been written. The *actual* number of cycles (ALV) it takes for a unit to become available is stored in the **functional unit**. This value is simply compared with the PLV value. If the unit becomes available sooner than PLV number of cycles, no action is necessary. If the unit is going to take longer than PLV number of cycles to become available, it asserts a stall signal to stall further execution until it does become available. The power latency register therefore frees the **functional unit** from having to dynamically monitor the instruction stream when it is in a low power state to watch for instructions that require response from the unit. This is significantly less complex than dynamically sensing the instructions. In the preferred embodiment, two downcounters and some combinational logic are required to implement this feature.

DEPR:
The **functional units** are interconnected by buses 102 and 104 which provide data, address and control information to the various **functional units**. Also included in the microprocessor 100 is a **power control** register 106. The **power control** register 106 includes a plurality of fields for storing values. These values can be set by software or during the manufacturing process. Each field corresponds to a respective **functional unit**. Each **power control** register field, such as field 108, adjusts the execution rate and therefore the power dissipation of the corresponding **functional unit**. This control is performed in a variety of ways as described further below. Each **power control** register field is coupled to the corresponding **functional unit** via a respective bus. For example, bus 110 couples the field 108 to the **functional unit** FU.sub.1 to provide the value stored therein to the **functional unit**. Buses 112, 114 and 116 similarly provide the contents of the other **power control** register fields to the remaining **functional units**. The **power control** register 106 can also include additional fields, which are not coupled to a **functional unit**, for future expansion of the microprocessor architecture or for global **power management control** of the microprocessor 100. These fields can be one or more bits in width depending upon the resolution of control desired.

DEPR:
The microprocessor 100 also includes a latency control register 118. This register 118 also includes a plurality of fields, with each field corresponding to a **functional unit**. As with the **power control** register fields, the fields of the latency control register are provided to the **functional units** via buses.

120, 122, 124 and 126. As will be described further below, with reference to FIGS. 10 and 11, the value stored in the latency control register field correspond to an assumption made by a compiler as to the number of clock cycles
required for the corresponding **functional unit** to become fully operational after the **functional unit** has been placed back online by writing a predetermined value to the corresponding **power control** register field. The operation of the latency control register fields will become more apparent in the description included herein below.

DEPR:
The clock divider 128 is coupled to a global **power control** register field 140 for receiving a value stored therein. This global register field 140 is not dedicated to a particular **functional unit** but instead adjusts the rate of execution of all the **functional units** by controlling the clock frequency supplied to all the **functional units**. The value stored in field 140 is provided to the clock divider 128 over bus 142. The clock divider divides down
the master clock signal responsive to the value stored in the **power control** register field 140. The clock divider divides the master clock signal down in accordance with the value stored in field 140. The extent to which the master clock signal is divided down depends upon the number of bits in the register field 140. In the preferred embodiment, the clock divider divides the master clock signal down by integer ratios (e.g., 1/2, 1/3, 1/4 . . . 1/16) responsive to a corresponding values stored in field 140. The amount of resolution is a function of the number of bits in the **power control** register fields and can thus be set by the designer. A predetermined value can also be used to divide the master clock signal down to zero.

DEPR:
This approach can be used for each **functional unit wherein the corresponding power control** register field would adjust the clock rate supplied to that particular **functional unit** such as shown in FIG. 4; however, most pipeline microprocessors require a single clock frequency throughout. For those implementations that do not require a unified clock signal, individual clock divider circuits can be used.

DEPR:
Referring now to FIG. 4, a second approach to adjusting the rate of execution of the **functional units** in order to adjust or reduce the power consumption is shown. In this approach, the clock signals provided to the individual **functional units** are gated responsive to the value stored in the corresponding **power control** register field. As in FIG. 3, clock generator 144 produces a master clock signal, but instead of dividing down the master clock signal, the clock signals that are provided to the individual **functional units** are gated by
an AND gate such as AND gate 146. AND gate 146 prevents the master clock signal from being distributed to the **functional unit** FU.sub.1 unless the value stored in the **power control** register fields 108 is all binary ones. In this way, the clock signal can be selectively applied and removed from the **functional unit** depending upon the value stored in the corresponding **power control** register field 108. It should be apparent that this approach is not limited to a value of all binary ones but rather this is the preferred embodiment given that no additional current logic is required to gate the clock
signal.

DEPR:

Referring now to FIG. 5, a different approach is shown for where the **functional unit** is an input/output (I/O) unit. In that case, the **functional unit** includes a logic block 148 that is coupled to the corresponding **power control** register field 108 to receive the value stored therein. The logic block 148 produces two outputs. The first is a clock divider output that is provided to a clock divider 150 such as that described in FIG. 3. The clock divider output of the logic block 148 is used by the clock divider 150 to determine the clock rate of the I/O.sub.-- CLK output of the clock divider. The I/O.sub.-- CLK signal is provided to a clock input of an output latch 152. The output latch is used to gate or latch the data output of the I/O **functional unit**. Thus, the I/O rate of the **functional unit** can be adjusted by changing the value stored in the corresponding **power control** register field 108. Therefore, the power dissipated by the **functional unit**, which is a function of the I/O rate, can be adjusted by varying the value in that field.

DEPR:
Yet another approach to reducing power in the individual **functional units** is shown in FIG. 6. In this approach, a transistor is interposed between the **functional unit** and a supply voltage terminal. This approach effectively reduces the rate of execution of the **functional unit** to zero by disabling that **functional unit**. As shown in FIG. 6, a transistor 158 is interposed between a ground terminal of the **functional unit** and the ground of the microprocessor. The gate of the transistor 158 is coupled to a logic block 160, which provides an enable signal to the gate of the transistor responsive to the value stored in the **power control** register field 108. In this approach, the **power control** register field needs simply be only a single bit wherein the logic reduces to a simple conductor. Where the **power control** register field is multiple bits, however, the logic 160 will be combinational logic that will decode the predetermined value and will deassert the enable signal when that value is detected. It should be apparent to those skilled in the art that the transistor can be interposed between the positive supply V.sub.dd and the positive supply input of the **functional unit** as well. As is shown in FIG. 6, each of the other **functional units** has a transistor associated therewith for controlling the rate of execution thereof. These transistors are responsive to the value stored in the corresponding field in the **power control** register. The corresponding logic blocks and various connections are not shown to simplify the drawing.

DEPR:
Referring now to FIG. 7, a different approach to adjusting the rate of execution of a **functional unit** responsive to the **power control** register field wherein that **functional unit** is a multiported memory is shown. Many microprocessors include multiported memories to allow for multiple concurrent accesses to the memory. Typically, these memories are used in register files or in cache memories. A two ported static random access memory (SRAM) 162 is shown in FIG. 7. Associated with each port (PORT.sub.1 and PORT.sub.2 is a sense amp, a driver, an address decoder and pull-up transistors, as is known in the art.

DEPR:
The logic block 164 also produces a second enable signal (ENABLE.sub.2), which

controls the components associated with the second port (PORT.sub.2) in an identical manner. The ENABLE.sub.1 and ENABLE.sub.2 signals can be asserted/deasserted responsive to the same or different values stored in the **power control** register depending on the number of bits and resolution in the field 108. Alternatively, different fields can be assigned to each memory port. By selectively enabling and disabling these components, the execution rate and therefore the power dissipation of the **functional unit** FU.sub.1 can be
adjusted accordingly.

DEPR:
A further approach that can be used to **control the amount of power** consumed by the microprocessor is shown in FIG. 8. In this approach, data is selectively removed from the **functional units** responsive to the value stored in the corresponding field in the **power control** register. This is accomplished by tri-stating or disabling a buffer that couples the data to the **functional unit**.
For example, as shown in FIG. 8, a data bus 170 is coupled to the various **functional units** via tri-state buffers such as buffer 172. A logic block 174 is coupled between the **power control** register field 108 corresponding to **functional unit** FU.sub.1 and the tri-state buffer 172. The logic block 174 selectively disables the buffer 172 by deasserting an enable signal ENABLE provided to the buffer responsive to a predetermined value detected in the register field 108. By disabling the buffer 172, the power consumed by charging and discharging the parasitic capacitances on bus 176 and the power consumed by the logic coupled to that bus can be reduced. This again can be thought of as adjusting the rate of execution of the **functional unit since the functional unit** cannot execute without data.

DEPR:
The logic block 178 generates the MUX signal responsive to the value stored in the **power control** register field 108 among other things. The **power control** register field 108 can therefore be used to switch the **functional unit**, and therefore the microprocessor, between a 32-bit and a 64-bit interface, which produces a corresponding change in the power consumption due to the reduced number of data lines that are driven. This is similar to the dynamic bus sizing techniques used, for example, in the Motorola 68040 microprocessor except that the bus sizing in the invention is done responsive to the value stored in the **power control** register and not to some external input provided to
the microprocessor.

DEPR:
Another aspect of the invention is shown in FIGS. 10 and 11. It should be apparent to those skilled in the art that depending upon which of the above-described approaches are used, the **functional unit** will not be immediately available or operational even after the corresponding **power control**
register field has been changed to place the **functional unit** in a full power or
normal power mode. For example, where power is reapplied to the **functional unit** by storing the appropriate value in the **power control** register field, it may be several clock cycles before the **functional unit** can execute or perform its function. Thus, if an instruction is issued to it prematurely, the result produced thereby will be erroneous. Accordingly, the invention includes the power latency register 118 and associated logic within the **functional unit** to stall the microprocessor pipeline in the event this condition occurs. This

approach differs from the prior art in that the **functional units** do not monitor
the instructions, which imposes a tremendous hardware burden on the **functional units**, but instead perform a simple comparison between an actual power latency register value stored in the **functional unit** and a corresponding power latency register field in the power latency register 118.

DEPR:
As shown in FIG. 10, each **functional unit** includes an actual power latency register and a stall logic block. The actual power latency register includes a
value that represents the actual number of clock cycles required for the **functional unit** to become fully operational after the **functional unit** has gone from a reduced operational state to a more fully operational state. As will be
apparent from the description above, this corresponds to the situation where the corresponding **power control** register field, which controls the rate of execution of the **functional unit**, changes from a value corresponding to a reduced power state and to one corresponding to a full power state. The corresponding field in the power latency register 118, on the other hand, corresponds to an assumption made by a compiler as to what the actual power latency register value is. The compiler uses this assumption to ensure that instructions are not issued to that **functional unit** before this number of cycles has expired after the corresponding **power control** register field has been changed to a full operational value. This offloads the responsibility of checking the instructions from the **functional unit** to the compiler. This is a superior approach to that of the prior art because the **functional units** need not dynamically monitor instructions. This approach is similar to that described in our co-pending, commonly-assigned application entitled "Method and
Apparatus for Simplifying Interlock Hardware," Ser. No. 08/059,041, filed May 6, 1993, incorporated herein by reference.

DEPR:
In FIG. 10, each **functional unit** is shown having an actual power latency register (APLR) and associated stall logic. For example, **functional unit** FU.sub.1 includes an actual power latency register 200 and associated logic 202. The stall logic 202 includes three inputs: one coupled to the register 200 to receive the actual power latency value, a second input coupled to the corresponding field in the power latency register 118 to receive the assumed latency value, and a third input coupled to the corresponding field 108 in the **power control** register 106. The stall logic needs to monitor the **power control**
register field 108 to detect when the value stored therein has been changed to the value corresponding to an increase in the operational state. In the preferred embodiment, this corresponds to the case where the **functional unit** is
placed into a fully operational or normal state. However, this value can correspond to any operational state or even a number of states in which the **functional unit** is operational.

DEPR:
The stall logic 202 produces a stall signal POWER.sub.-- STALL.sub.1 that is provided to a pipeline control unit 204 that controls a multistage pipeline in the microprocessor. The signal line 206 provides this power stall signal to the pipeline control unit 204. The stall logic asserts the power stall signal POWER.sub.-- STALL.sub.1 where the compiler has made an erroneous assumption about the actual power latency value. This signal remains asserted until the

required number of cycles have expired, as specified by the actual power latency register value, after the corresponding **power control** register field 108 has been changed from a low power or reduced power value to a fully or normal operational value. The other **functional units** also produce power stall signals (POWER.sub.-- STALL.sub.2 . . . POWER.sub.-- STALL.sub.n) under similar conditions.

DEPR:
The microprocessor 100 with the **power control** register and the associated means
for adjusting the rate of the execution units allows software to adjust or **control the power** dissipation of the microprocessor. This is advantageous over
hardware because software can look much further into the future to determine what function units will be required in the future. Those that will not be required can be set to a low power or no power state by setting the appropriate
value in the corresponding **power control** register field. This capability further allows the software to attempt to keep the power dissipation below a predetermined amount by serializing tasks that could otherwise be done in parallel. Although this would reduce the performance of the microprocessor, it
would help to reduce power, thereby allowing the same silicon die to be used in
a variety of different packages including low cost plastic packages or those without heat sinks. Certain **functional units** could even be permanently disabled or put into a low power state by setting the value during manufacturing of or the wafer or packaging of the part to ensure that the silicon did not dissipate more power than is allowed for the package. The software could then sense this setting and serialize the task accordingly.

CLPR:
7. A microprocessor according to claim 1 wherein the **power control** logic circuitry includes a transistor interposed between one of the subset of **functional units** and a supply voltage terminal such that the transistor isolates the supply voltage terminal from the one of the subset of **functional units** responsive to the value in the corresponding power register field.

CLPR:
8. A microprocessor according to claim 1 wherein the **power control** logic circuitry includes a buffer circuit which disables transitions on data inputs to the **functional unit** responsive to the value stored in the corresponding power register field.

CLPR:
9. A microprocessor according to claim 1 further including a clocking circuit for generating a clock signal and supplying said clock signal to the **functional**
units, wherein the power control logic circuitry includes a clock divider circuit interposed between the clocking circuit and one of the subset of **functional units** such that the clock divider circuit divides the clock signal responsive to the value in the power register field corresponding to the one of
the subset of **functional units**.

CLPR:
11. A microprocessor according to claim 1 further including a power latency register having a latency field for storing a latency value corresponding to a

number of clock cycles after the value stored in a corresponding power register
field has been adjusted that a compiler assumes that the **functional unit** corresponding to the power register field is available, the **functional unit** including means for stalling its execution until the **functional unit** is available after the value stored in the corresponding power register field in the **power control** register has been changed to place the **functional unit** in a normal state.

CLPR:
14. A computer according to claim 13 wherein the microprocessor includes a clocking circuit that generates a clock signal that is provided to at least one
of the plurality of **functional units, and wherein the power control** logic circuitry includes a clock divider circuit interposed one of the **functional units** and the clocking circuit and configured to divide the clock signal responsive to the value in the power register field corresponding to the **functional unit**.

CLPR:
23. A method of minimizing power consumption according to claim 20, wherein storing a **power control** value in the microprocessor includes storing a value for each **functional unit in a power control** register.

CLPR:
25. A method of minimizing power consumption according to claim 24, including storing a **power latency value and controlling** the adjusting of the rate of execution of the selected **functional unit** to full power according to the power latency value.

CLPR:
32. A method for **controlling power** consumption of a plurality of **functional units** in a microprocessor, the method comprising:

CLPR:
33. The method of claim 32, wherein setting the value in each one of the fields of the **power control** register includes determining the value in each field of the **power control** register based upon whether the corresponding one of
the plurality of **functional units** is utilized in a code segment to be executed.

CLPR:
34. The method of claim 33, wherein determining the value in each field of the
power control register includes setting the value in each field of the **power control** register to stop a clock signal input to the corresponding one of the plurality of **functional units** is not utilized in the code segment to be executed.

CLPR:
35. The method of claim 34, wherein determining the value in each field of the
power control register includes setting the value in each field of the **power control** register to restore the clock signal input to the corresponding one of the plurality of **functional units** in advance of when the **functional unit** is to be utilized in the code segment to be executed.

CLPR:
36. The method of claim 35, wherein the step of setting the value in each field of the **power control** register to restore the clock signal includes restoring the clock signal in advance of when the **functional unit** is to be utilized in the code segment to be executed by a predetermined latency period of the **functional unit**.

CLPV:
a power register within the microprocessor having a plurality of power register
fields, each power register field uniquely corresponding to a **functional unit** of the subset of **functional units** having variable execution rates, wherein each
one of the plurality of power register fields is configured to receive and store a **power control** value for its corresponding **functional unit** responsive to
one of the series of instructions; and

CLPV:
power control logic circuitry within the microprocessor coupled to the power register and configured to adjust the rate of execution of each individual **functional unit** of the subset of **functional units** having variable execution rates responsive to the **power control value stored in the power** register field uniquely corresponding to that individual **functional unit** so that the power dissipated by each **functional unit** of the subset of **functional units** having variable execution rates is individually determined solely by the **power control**
value stored in its corresponding power register field.

CLPV:
a microprocessor having a plurality of **functional units** within the microprocessor, a **power control** register within the microprocessor having a plurality of power register fields, each field corresponding to a corresponding
one of the **functional units**;

CLPV:
executable code stored in the memory, the microprocessor being responsive to the code to store values in each of the power register fields for individually **controlling the level of power** consumption of one of the **functional units** according to its corresponding power register field; and

CLPV:
power control logic circuitry configured to independently adjust the rate of execution of each one of the **functional units** having a corresponding power register field responsive to the value stored in the corresponding power register field so that the power dissipated by each of the **functional units** is independently adjusted by the value stored in the corresponding power register field.

CLPV:
a microprocessor having a plurality of **functional units** within the microprocessor, a **power control** register within the microprocessor having a plurality of **power control** register fields, each field corresponding to a corresponding one of the **functional units**;

CLPV:
executable code stored in the memory, the microprocessor being responsive to the code to store values in the **power control** register fields for independently
controlling the level of power consumption of the corresponding **functional units**;

CLPV:
power control logic circuitry configured to adjust the rate of execution of each one of the **functional units having a corresponding power control** register field responsive to the value stored in the corresponding **power control** register field so that the power dissipated by the corresponding **functional unit** is independently adjusted by the value in the corresponding **power control** register; and

CLPV:
providing the microprocessor with a **power control** register within the microprocessor having a plurality of fields, each field corresponding to a **functional unit**;

CLPV:
providing the microprocessor with a **power control** register within the microprocessor having a plurality of fields, each field corresponding to a **functional unit**;

CLPV:
coupling **power control** circuitry to the plurality of **functional units, the power control** circuitry being adapted to individually adjust the power consumption of each one of the plurality of **functional units**;

CLPV:
coupling a **power control** register having a plurality of fields to the **power control** circuitry, where each one of the plurality of field of the **power control** register corresponds to one of the plurality of **functional units**;

CLPV:
independently adjusting the power consumption of each one of the plurality of **functional units** responsive to a value in the corresponding field of the **power control** register; and

CCOR:
713/322

CCXR:
713/324

US-CL-CURRENT: 710/14,710/8 ,710/9 ,**713/323**

US-PAT-NO: 5832280
DOCUMENT-IDENTIFIER: US 5832280 A
TITLE: Method and system in a data processing system for interfacing an operating system with a power management controller.
DATE-ISSUED: November 3, 1998
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swanberg; Randal Craig	Round Rock	TX	N/A	N/A

US-CL-CURRENT: **713/300**,710/14 ,710/8 ,710/9 ,**713/323**

ABSTRACT:
In a data processing system having an operating system and a power management controller coupled to one or more power-managed devices, each of the
power-managed devices is assigned a device identifier. An architected power-managed device select register and an architected power mode select register are provided within the data processing system. To modify a power mode of a power-managed device, the operating system writes a selected one of the device identifiers to the architected power-managed device select register for selecting an identified one of the power-managed devices. Thereafter, the operating system writes a power mode identifier to the architect power mode select register for selecting one of a plurality of power modes within the selected power-managed device. The device identifier and the power mode identifier are translated into control signals for the power management controller within the data processing system. Such control signals are then transmitted to the power management controller and the identified power-managed
device is operated in the selected power mode, wherein the operating system controls the power modes of power-managed devices without programming a particular implementation of power management control in the operating system.
10 Claims, 5 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

BSPR:
The **control of power** consumption within a data processing system has become increasingly important, particularly since portable data processing systems that use a self-contained power source have become popular. Such a self-contained power source is typically a battery. In order to maximize the amount of data processing that may be done using the power stored in a reasonably sized battery, various **functional units** within the data processing system may be disconnected from the battery power source, or operated in a lower power consuming mode, until the full function of a particular unit is needed. Examples of such **functional units** include hard disk drives, floppy disk drives, modems, display devices, CD-ROM drives, and the like. Each of these devices may be designed to operate in a plurality of power modes. For example, a simple set of power modes may include a "power on" mode and a "power
off" mode. Other power modes may include a low power mode that retains the state of the **functional unit** in memory, a low power mode that retains a partial
state of the **functional unit**, and a low power mode that does not retain any state of the **functional unit**.

BSPR:

In the prior art, various integrated circuits, called **power management controllers, control the power** modes of one or more **functional units** within a data processing system. For example, one **power management controller** is sold under the part number "83C750" by Philips Components--Signetics, and another **power management controller** is sold under the part number "50753" by Mitsubishi
Corporation. For more information on the 83C750, see the publication entitled "Philip Components--Signetics Products Specification".

BSPR:
Such **power management controllers typically control the power** supplied to various **functional units** within the data processing system, and may further control the frequency of a clock signal supplied to each **functional unit** in order to reduce the power consumed by that **functional unit**.

BSPR:
To **control the power** management unit, the operating system in the data processing system writes command words into **control registers within the power management controller**. Such control registers may be located at any address in
addressable memory space that is reserved for input/output. Thus, an operating
system in the prior art, which may be designed to operate on different hardware
platforms, must be programmed to write to the **power management control** registers at the proper I/O address for each data processing system hardware platform. The operating system must be programmed in different ways to operate
in different hardware platforms because each data processing system may include
different **functional units, and such functional units** may be connected to the **power management controller** in different ways.

BSPR:
Furthermore, different **power management controllers** may require different commands and control signals to perform similar functions. This means that the
operating system must also be programmed to operate the selected **power management controller** used in the design of the particular data processing system. Therefore, the problem in the prior art with using the operating system to **control functional unit power** modes is that the operating system must
be particularly programmed for each different hardware platform that uses a **power management controller**. This means that prior art operating systems that manage power modes in **functional units** (i.e., power managed devices) are not truly portable between hardware platforms--some reprogramming of the operating system/power management controller interface is necessary.

DEPR:
Those persons skilled in the art of data processing systems design should recognize that display 26, keyboard 24, and pointing device 32 may each be implemented utilizing any one of several known off-the-shelf components. Data processing system 20 may be implemented utilizing any general purpose computer or so-called personal computer that utilizes an operating system to **control power** modes of **functional units** in the computer through a **power management controller**. An example of such a general purpose computer is the computer sold

under the trademark "RS/6000" by International Business Machines Corporation (IBM), of Armonk, N.Y. An example of such a personal computer is the personal computer sold under the trademark "PS/2".

DEPR:
With reference now to FIG. 3, there is depicted a high-level block diagram which further illustrates the configuration of a **power management controller and power**-managed devices within a data processing system in accordance with the method and system of the present invention. As illustrated, CPU 50 is connected to system bus 54. Also coupled to system bus 54 is system memory 120, which may be utilized to store at least a portion of operating system 122.
Operating system 122 is the software responsible for controlling the allocation
and usage of hardware resources such as memory, central processing unit (CPU) time, disk space, and peripheral devices or **functional units**. Operating system
122 is the foundation on which applications such as word-processing and spreadsheet programs are built. Examples of operating systems include the operating system sold under the trademark "MS-DOS" by Microsoft Corporation and
the operating system sold under the trademark "AIX" by International Business Machines.

CCOR:
713/300

CCXR:
713/323

US-CL-CURRENT: **713/320**

US-PAT-NO: 5828568
DOCUMENT-IDENTIFIER: US 5828568 A
TITLE: Information processing apparatus, processing method thereof, and power supply control method therefor
DATE-ISSUED: October 27, 1998
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sunakawa; Shinichi	Kawasaki	N/A	N/A	JPX
Shimada; Kazutoshi	Yokosuka	N/A	N/A	JPX
Tatsumi; Eisaku	Kawasaki	N/A	N/A	JPX
Mori; Shigeki	Koshigaya	N/A	N/A	JPX
Matsubayashi; Kazuhiro	Yokohama	N/A	N/A	JPX
Harada; Takashi	Yokohama	N/A	N/A	JPX
Nagasaki; Katsuhiko	Ichikawa	N/A	N/A	JPX
Fukuda; Ryoji	Yokohama	N/A	N/A	JPX

US-CL-CURRENT: 700/79,**713/320**
ABSTRACT:

An information processing apparatus, which operates in a multi-task mode, calculates a total consumption power of devices used by each task, and assigns higher execution priority to a task which uses a device with the largest consumption power, thereby shortening the execution time of the device with the largest consumption power, and suppressing the total consumption power of the apparatus. When a device is started upon switching of tasks, if the total consumption power exceeds the allowable power of the apparatus by a power consumed upon restarting of the device, the task is set in a waiting state until operations of other devices are completed, the consumption power is lowered, and it is ready to use the device by the task.

32 Claims, 30 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 25

DEPR:
Power is supplied to these **functional units** via switches 21 to 26 included in the **power supply controller** 4. These switches 21 to 26 have a one-to-one correspondence with the above-mentioned units. When a corresponding switch is turned off, power supply to the unit is stopped, and its processing can also be stopped. The ON/OFF control of these switches is executed by the CPU 1 via the CPU peripheral circuit 2.

CCXR:
713/320

US-CL-CURRENT: 712/242,712/243 ,713/321 ,713/323 ,713/601

US-PAT-NO: 5815724
DOCUMENT-IDENTIFIER: US 5815724 A
TITLE: Method and apparatus for controlling power consumption in a microprocessor
DATE-ISSUED: September 29, 1998
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mates; John William Benson	Portland	OR	N/A	N/A

US-CL-CURRENT: 713/322,712/242 ,712/243 ,713/321 ,713/323 ,713/601

ABSTRACT:
A system for controlling power consumption in a microprocessor. The microprocessor fetches an instruction from memory. The instruction is decoded,
producing an operation flow of at least one operation. Then, power micro-operations are introduced into the operation flow. These power micro-operations provide power consumption control functions for those functional units which are required to execute the various operations which have been decoded from the fetched instruction. The operations and power micro-operations are then scheduled for dispatch to the appropriate execution units. The scheduling is based on the availability of the appropriate execution units and the validity of operation data. The operations and power micro-operations are dispatched to the appropriate execution units, where the operations and power micro-operations are executed. The execution results are subsequently committed to the processor state in the original program order.
24 Claims, 4 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 4

ABPL:
A system for controlling power consumption in a microprocessor. The microprocessor fetches an instruction from memory. The instruction is decoded,
producing an operation flow of at least one operation. Then, power micro-operations are introduced into the operation flow. These power micro-operations provide power consumption control functions for those functional units which are required to execute the various operations which have been decoded from the fetched instruction. The operations and power micro-operations are then scheduled for dispatch to the appropriate execution units. The scheduling is based on the availability of the appropriate execution units and the validity of operation data. The operations and power micro-operations are dispatched to the appropriate execution units, where the operations and power micro-operations are executed. The execution results are subsequently committed to the processor state in the original program order.

BSPR:
Another method for controlling power consumption in a microprocessor includes placing circuitry throughout the microprocessor that tracks events that occur within the microprocessor. The circuitry is designed to detect the occurrence of certain events within the microprocessor, and to take steps to perform power
management functions, typically shutting down a clock signal feeding a particular functional unit within the microprocessor.

DEPR:
Although the following embodiment is described using a floating point addition instruction and a floating point execution unit, the present invention may be practiced with other types of instructions and **functional units** as well. For example, the present invention may be practiced to enable a **functional unit** that accesses memory when an instruction is decoded that requires a memory access. In this manner, a microprocessor implemented in accordance with the present invention can efficiently **control power** consumption, since only the required **functional units** are enabled at a given time. Further, the present invention may be practiced to offer other types of **power consumption control to the functional units** other than turning the units on or off.

DEPR:
FIG. 1 depicts one embodiment of a method for fetching, decoding, executing, and writing results in accordance with the present invention. The method of FIG. 1 includes the insertion of power micro-operations, or P.mu.Ops, into the operation flow. The P.mu.Ops provide system-transparent **power management control** functions which enable and disable various **functional units** depending on the requirements of the operation flow. Referring again to FIG. 1, in the Fetch Instruction step 110, a macroinstruction is fetched from memory . In this example, the macroinstruction fetched is FADD m32 real, which adds a 32 bit floating point number stored in memory to a 32 bit floating point number stored on top of the stack, and stores the results on top of the stack. Once the macroinstruction is fetched from memory, it is decoded at the Decode Instruction/Insert P.mu.Ops step 120. At this step, the FADD m32 real macroinstruction is broken down into a number of micro-operations (.mu.Ops). In this example, the .mu.Ops specify that the contents of the stack be placed in a floating point register FPR1, that the contents of memory location m32 real be moved to another floating point register FPR2, that the contents of FPR1 and FPR2 be added, and that the results of the addition are stored on top of the stack. In addition, two P.mu.Ops are inserted into the operation flow. To determine which P.mu.Ops to insert, at the Decode Instruction/Insert P.mu.Ops step 120, the macroinstruction is examined to determine which **functional units** are required in order to execute the decoded macroinstruction.
For example, the P.mu.Ops specify that the Floating Point Execution Unit (FEU) is turned on before the floating point addition occurs and turned off again after the floating point addition has completed.

DEPR:
In one embodiment, the power unit 345 executes the P.mu.Ops by enabling or disabling clock signals that are coupled to other **functional units** throughout the microprocessor. These other **functional units** may include but are not limited to the FEU, IEU, MIU, and AGU. The power unit 345 may also be implemented to control clock signals which are coupled to registers, queues, caches, etc., thereby allowing the **Power Unit to control power** consumption in any unused or unneeded **functional units**. By disabling clock signals, the power
consumed in the disabled **functional units** is dramatically reduced.

CLPR:
4. The method for **controlling power** consumption in a microprocessor of claim 3, wherein the step of scheduling the operation and power micro-operation for dispatch further includes scheduling the power micro-operation such that the appropriate **functional units** are enabled before the corresponding operation is executed and are disabled after the corresponding operation has been executed.

CLPR:
6. The method for **controlling power** consumption in a microprocessor of claim 5, wherein the power unit executes the power micro-operation through manipulation of a plurality of clock signals coupled to the **functional units**.

CLPV:
inserting at least one power micro-operation into the operation flow, the power
micro-operation providing **power consumption control** for at least one **functional**
unit required to execute the operation, the power micro-operation in addition to the operation provided by decoding the instruction;

CLPV:
means for inserting at least one power micro-operation into the operation flow,
the power micro-operation providing **power consumption control** for at least one **functional unit** required to execute the instruction, the power micro-operation in addition to the operation provided by decoding the instruction;

CLPV:
an instruction decoder receiving at least one instruction, the instruction decoder producing at least one operation for each instruction, said instruction
decoder further producing at least one power micro-operation providing **power consumption control** for at least one **functional unit** required to execute the operation, the power micro-operation in addition to the operation provided by decoding the instruction; and

CCOR:
713/322

CCXR:
713/321

CCXR:
713/323

CCXR:
713/601

US-CL-CURRENT: 713/310,713/321 ,713/324

US-PAT-NO: 5787297
DOCUMENT-IDENTIFIER: US 5787297 A
TITLE: Selective power-down for high performance CPU/system
DATE-ISSUED: July 28, 1998
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Chong Ming	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 713/322,713/310 ,713/321 ,713/324
ABSTRACT:

A microelectronic device according to the present invention is made up of two or more functional units, which are all disposed on a single chip, or die. The present invention works on the strategy that all of the functional units on the die are not, and do not need to be operational at a given time in the execution of a computer program that is controlling the microelectronic device. The present invention on a very rapid basis (typically a half clock cycle), therefore, turns on and off the functional units of the microelectronic device in accordance with the requirements of the program being executed. This power down can be achieved by one of three techniques; turning off clock inputs to the functional units, interrupting the supply of power to the functional units, or deactivating input signals to the functional units. The operation of the present invention results in a very significant reduction in power consumption and corresponding heat dissipation by the microelectronic device as compared to the conventional approach of keeping all functional units operational all of the time.

12 Claims, 9 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 6

DEPR:
The present invention is a system and method for selectively **controlling the power provided to each of the functional units** of a microelectronic device so that the **functional units** can be turned on and off as needed by the execution of the computer program that is controlling the microelectronic device. The dynamic turning on and off of the **functional units** in accordance with the requirements of the program step(s) being executed causes a significant reduction in power (e.g., 10-30%) consumed by the **functional units**, which results in significant reduction in the heat dissipation requirements and a significant reduction in the power requirements of the microelectronic device. The present invention results in significant reduction in heat dissipation requirements and in power requirements for the microelectronic device, which means that heat sink requirements are reduced and battery discharge cycle length is extended, both of which are very desirable results. In addition, power bus line widths can be reduced. This leads to substantial area saving for VLSI chips.

DEPR:
Coupling/decoupling of a power supply bus is also envisioned. The addition of a power switch(es) connected between V.sub.DD and each **functional unit**, can be used to turn on and off the supply of **power to the functional units by controlling the power** switch (e.g., FET) using the above CKPWRON control

signal, or the like. In this power-down case, some DC power will be consumed through the power switch, but with the **functional unit**(s) disconnected, overall
conservation will result.

CLPV:
(e) first logic means, coupled to said instruction decoding unit and said one or more **power switches, for controlling the supplying of power** from the power supply to the **functional unit** needed to execute said machine code instruction so that power is supplied a second preselected number of system clock cycles before said machine code instruction is executed; and

CLPV:
(f) second logic means, coupled to said instruction execution unit, said first logic means, and said one or more **power switches, for controlling the supplying**
of power from the power supply to the **functional unit** executing said machine code instruction so that power is supplied until the execution of said machine code instruction is complete as determined by said instruction execution unit, whereby the power consumption of said microelectronic device is reduced.

CCOR:
713/322

CCXR:
713/310

CCXR:
713/321

CCXR:
713/324

US-CL-CURRENT: 700/286,713/300 ,713/322 ,713/323 ,713/601

US-PAT-NO: 5737616
DOCUMENT-IDENTIFIER: US 5737616 A
TITLE: Power supply circuit with power saving capability
DATE-ISSUED: April 7, 1998
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Watanabe; Mitsuhiro	Tokyo	N/A	N/A	JPX

US-CL-CURRENT: 713/340,700/286 ,713/300 ,713/322 ,713/323 ,713/601

ABSTRACT:
A power supply circuit efficiently saves electric energy consumed by a central processing unit and a peripheral assembly through coordination between power supply modes of the central processing unit and the peripheral assembly. The central processing unit has a register for establishing a status of an internal power supply of the central processing unit, a first mechanism for changing the internal power supply into the status established by the register,
and a second mechanism for outputting a status signal indicative of the status.
The peripheral assembly having a peripheral circuit, a peripheral device, and a
power supply control block for changing power supply statuses and clock statuses of the peripheral circuit and the peripheral device based on the status signal outputted from the second mechanism.
8 Claims, 11 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 10

BSPR:
Various attempts have been made to realize the second alternative. For example, Japanese laid-open patent publication No. 60-254487 discloses a method
of suppressing the consumption of electric energy by a semiconductor integrated
circuit by shutting down the circuit with a power-down mechanism incorporated in the circuit which operates in response to an external power-down signal. According to a power saving method revealed in Japanese laid-open patent publication No. 2-201516, a **power control** register is accessible by a CPU, and a switch means can permit and inhibit the supply of electric energy to a clock generator depending on the state of a predetermined bit in the **power control** register, so that the consumption of electric energy is reduced by setting the bit to a given value in the **power control** register. Japanese laid-open patent publication No. 5-324139 shows a **power-down control** method for controlling the individual supply of electric energy to a plurality of **functional units** including a CPU with a **power-saving control** register.

CCOR:
713/340

CCXR:
713/300

CCXR:
713/322

CCXR:
713/323

CCXR:
713/601

US-CL-CURRENT: 713/322,713/323

US-PAT-NO: 5719800
DOCUMENT-IDENTIFIER: US 5719800 A
TITLE: Performance throttling to reduce IC power consumption
DATE-ISSUED: February 17, 1998
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mittal; Millind	South San	CA	N/A	N/A
Valentine; Robert	Francisco	N/A	N/A	ILX
	Qiryat Tivon			

US-CL-CURRENT: 713/321,713/322 ,713/323

ABSTRACT:
The power consumed within an integrated circuit (IC) is reduced without substantial impact on its performance for typical applications by throttling the performance of particular functional units within the IC. Artificial worst-case power consumption is reduced by throttling down the activity levels of long-duration sequences of high-power operations. The recent utilization levels of particular functional units within an IC are monitored--for example, by computing each functional unit's average duty cycle over its recent operating history. If this activity level is greater than a threshold, then the functional unit is operated in a reduced-power mode. The threshold value is set large enough to allow short bursts of high utilization to occur without impacting performance. The invention allows an integrated circuit to dynamically make the tradeoff between high-speed operation and low-power operation, by throttling back performance of localized functional units when their utilization exceeds a sustainable level. Additionally, this dynamic power/speed tradeoff can be optimized across multiple functional units within an IC or among multiple ICs within a system. Additionally, this dynamic power/speed tradeoff can be altered by providing software control over throttling parameters.
32 Claims, 6 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

BSPR:
The invention relates generally to reducing the power consumption of Integrated
Circuits (ICs), and particularly of Very Large Scale Integration (VLSI) ICs. In particular, it relates to methods and apparatus for throttling the performance of particular **functional units** within an IC as needed to **control worst-case power** consumption.

BSPR:
Within any IC, a number of particular **functional units** can consume inordinate amounts of power. For example, floating-point arithmetic units and cache memories are two types of **functional units** within a microprocessor IC that can consume substantial amounts of power. The invention allows IC designers to identify any number of such high-power **functional units** within the IC they are designing, and place each under the **control of its own power controller**. Further, the invention allows IC designers to place the IC they are designing as a whole under the **control of an overall power controller**. In the case of a microprocessor IC, the power consumption as a whole can effectively be throttled by lowering either the instruction retirement rate or the instruction
issue rate.

BSPR:
In one embodiment, the **power controller** comprises an activity monitor and a mode controller. The activity monitor tracks the recent utilization level of a particular **functional unit** within the IC--for example, by computing its average duty cycle over its recent operating history. If this activity level is greater than a threshold, then the mode controller switches the **functional unit** to operate in a reduced-power mode. The threshold value is set large enough to allow short bursts of high utilization to occur without impacting performance.

DEPR:
The invention is flexible in that it encompasses a wide range of design alternatives for reducing the **power of the functional unit that it controls**. These design alternatives can range from very simple to quite complex. In fact, each **functional unit controlled may have a different power** reduction technique for which it is most suited.

DEPR:
Integrated circuit #1 may include a number of additional **functional units,** like **Functional Unit** #3, whose **power consumption is not controlled--perhaps because the power** consumed is relatively small, or there is no cost-effective technique for **controlling its power** consumption, or there is a very substantial performance impact of reducing its power consumption that makes it an unlikely candidate for such control.

DEPR:
As shown in IC #1 in FIG. 5, **functional units** #1 and #2 have an associated activity monitor & mode controller 502. **Functional unit** #3 has an associated activity monitor 504, but no mode controller. **Functional unit** #4 has an associated mode controller 505, but no activity monitor. Activity monitor & mode controller 502, activity monitor 504 and mode controller 505 are different types of local **power controllers,** whose operation is coordinated by power coordinator 503 altering their throttling parameters.

DEPR:
For example, **functional unit** #1 could be an instruction cache and **functional unit** #2 could be a data cache, each with an associated activity monitor and **power controller,** similar to that shown in FIG. 3. **Functional unit** #3 could be a floating-point arithmetic unit. **Functional unit** #4 could be the unit that performs instruction cache prefetching, as discussed in conjunction with FIG. 4.

CLPV:
a plurality of local **power controllers,** each associated with at least one of said **functional units** and each having throttling parameters, operable to **control the power** consumption of said associated **functional unit** in accordance with the current values of said throttling parameters; and

CCOR:
713/321

CCXR:
713/322

CCXR:
713/323

US-CL-CURRENT: 712/32

US-PAT-NO: 5666537
DOCUMENT-IDENTIFIER: US 5666537 A
TITLE: Power down scheme for idle processor components
DATE-ISSUED: September 9, 1997
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Debnath; Kathakali	Beaverton	OR	N/A	N/A
Sah; Anurag	Aloha	OR	N/A	N/A
Khieu; Cong Quoc	San Jose	CA	N/A	N/A

US-CL-CURRENT: **713/322**,712/32
ABSTRACT:

Power down circuitry in a processor for **controlling power** delivered to **functional units** of the processor, comprising first and second power down circuits. The first power down circuit comprises a state machine having a decoded instruction as input and a control signal as output. The control signal disables a clock signal to a floating point unit (FPU) when the decoded instruction is not a floating point instruction. The second power down circuit
comprises a prediction circuit that generates a predict signal when a cache access cannot occur. The predict signal disables a clock signal to a cache.
11 Claims, 6 Drawing figures
Exemplary Claim Number: 5
Number of Drawing Sheets: 6

ABPL:
Power down circuitry in a processor for **controlling power** delivered to **functional units** of the processor, comprising first and second power down circuits. The first power down circuit comprises a state machine having a decoded instruction as input and a control signal as output. The control signal disables a clock signal to a floating point unit (FPU) when the decoded instruction is not a floating point instruction. The second power down circuit
comprises a prediction circuit that generates a predict signal when a cache access cannot occur. The predict signal disables a clock signal to a cache.

CLPR:
1. In a processor, **power down circuitry for controlling power** delivered to **functional units** of the processor, comprising:

CCOR:
713/322

US-CL-CURRENT: 713/321,713/324

US-PAT-NO: 5655124
DOCUMENT-IDENTIFIER: US 5655124 A
TITLE: Selective power-down for high performance CPU/system
DATE-ISSUED: August 5, 1997
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Chong Ming	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 713/322,713/321 ,713/324
ABSTRACT:

A microelectronic device according to the present invention is made up of two or more functional units, which are all disposed on a single chip, or die. The present invention works on the strategy that all of the functional units on the die are not, and do not need to be operational at a given time in the execution of a computer program that is controlling the microelectronic device. The present invention on a very rapid basis (typically a half clock cycle), therefore, turns on and off the functional units of the microelectronic device in accordance with the requirements of the program being executed. This power down can be achieved by one of three techniques; turning off clock inputs to the functional units, interrupting the supply of power to the functional units, or deactivating input signals to the functional units. The operation of the present invention results in a very significant reduction in power consumption and corresponding heat dissipation by the microelectronic device as compared to the conventional approach of keeping all functional units operational all of the time.

20 Claims, 9 Drawing figures
Exemplary Claim Number: 11
Number of Drawing Sheets: 6

DEPR:
The present invention is a system and method for selectively **controlling the power provided to each of the functional units** of a microelectronic device so that the **functional units** can be turned on and off as needed by the execution of the computer program that is controlling the microelectronic device. The dynamic turning on and off of the **functional units** in accordance with the requirements of the program step(s) being executed causes a significant reduction in power (e.g., 10-30%) consumed by the **functional units**, which results in significant reduction in the heat dissipation requirements and a significant reduction in the power requirements of the microelectronic device. The present invention results in significant reduction in heat dissipation requirements and in power requirements for the microelectronic device, which means that heat sink requirements are reduced and battery discharge cycle length is extended, both of which are very desirable results. In addition, power bus line widths can be reduced. This leads to substantial area saving for VLSI chips.

DEPR:
Coupling/decoupling of a power supply bus is also envisioned. The addition of a power switch(es) connected between V.sub.DD and each **functional unit**, can be used to turn on and off the supply of **power to the functional units by controlling the power** switch (e.g., FET) using the above CKPWRON control

signal, or the like. In this power-down case, some DC power will be consumed through the power switch, but with the **functional unit**(s) disconnected, overall
conservation will result.

CLPV:
(d) logic means, coupled to said examining means, the at least two **functional units** and said one or more **power switches, for controlling the supplying of power** from the power supply to the at least two **functional units** so that power on said preselected cycle basis is supplied only to each of the **functional units** need to perform an operation in conjunction with executing said machine code instruction.

CCOR:
713/322

CCXR:
713/321

CCXR:
713/324

US-PAT-NO: 5452401
DOCUMENT-IDENTIFIER: US 5452401 A
TITLE: Selective power-down for high performance CPU/system
DATE-ISSUED: September 19, 1995
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Chong M.	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: 713/322

ABSTRACT:
A microelectronic device according to the present invention is made up of two or more functional units, which are all disposed on a single chip, or die. The present invention works on the strategy that all of the functional units on the die are not, and do not need to be operational at a given time in the execution of a computer program that is controlling the microelectronic device.
The present invention on a very rapid basis (typically a half clock cycle), therefore, turns on and off the functional units of the microelectronic device in accordance with the requirements of the program being executed. This power down can be achieved by one of three techniques; turning off clock inputs to the functional units, interrupting the supply of power to the functional units, or deactivating input signals to the functional units. The operation of the present invention results in a very significant reduction in power consumption and corresponding heat dissipation by the microelectronic device as compared to the conventional approach of keeping all functional units operational all of the time.
18 Claims, 10 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

DEPR:
The present invention is a system and method for selectively **controlling the power provided to each of the functional units** of a microelectronic device so that the **functional units** can be turned on and off as needed by the execution of the computer program that is controlling the microelectronic device. The dynamic turning on and off of the **functional units** in accordance with the requirements of the program step(s) being executed causes a significant reduction in power (e.g., 10-30%) consumed by the **functional units**, which results in significant reduction in the heat dissipation requirements and a significant reduction in the power requirements of the microelectronic device. The present invention results in significant reduction in heat dissipation requirements and in power requirements for the microelectronic device, which means that heat sink requirements are reduced and battery discharge cycle length is extended, both of which are very desirable results. In addition, power bus line widths can be reduced. This leads to substantial area saving for VLSI chips.

DEPR:
Coupling/decoupling of a power supply bus is also envisioned. The addition of a power switch(es) connected between V.sub.DD and each **functional unit**, can be used to turn on and off the supply of **power to the functional units by controlling the power** switch (e.g., FET) using the above CKPWRON control signal, or the like. In this power-down case, some DC power will be consumed through the power switch, but with the **functional unit**(s) disconnected, overall

conservation will result.

CLPV:
(d) logic means, coupled to said examining means, the at least two **functional units** and said one or more power switches and in communication with said machine code instruction, for **controlling the supplying of power** from the power
supply to the at least two **functional units,** so that power on said preselected cycle basis is supplied only to each of the **functional units** need to perform an
operation in conjunction with executing said machine code instruction.

CCOR:
713/322

L Number	Hits	Search Text	DB	Time stamp
1	9002	functional adj2 unit$1	USPAT; US-PGPUB	2001/12/27 16:19
4	135652	power near3 control$5	USPAT; US-PGPUB	2001/12/27 16:20
7	26606	(insert$3 or add$3) with (program$3 or (instruction adj stream$1))	USPAT; US-PGPUB	2001/12/27 16:22
10	0	(functional adj2 unit$1) same (power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))	USPAT; US-PGPUB	2001/12/27 16:22
13	108	(functional adj2 unit$1) same (power near3 control$5)	USPAT; US-PGPUB	2001/12/27 16:22
16	9257	713/$.ccls.	USPAT; US-PGPUB	2001/12/27 16:22
22	5	((functional adj2 unit$1) same (power near3 control$5)) and ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))	USPAT; US-PGPUB	2001/12/27 16:23
19	22	713/$.ccls. and ((functional adj2 unit$1) same (power near3 control$5))	USPAT; US-PGPUB	2001/12/27 16:28

L Number	Hits	Search Text	DB	Time stamp
1	9002	functional adj2 unit$1	USPAT; US-PGPUB	2001/12/27 16:46
4	135652	power near3 control$5	USPAT; US-PGPUB	2001/12/27 16:46
7	26606	(insert$3 or add$3) with (program$3 or (instruction adj stream$1))	USPAT; US-PGPUB	2001/12/27 16:46
10	0	(functional adj2 unit$1) same (power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))	USPAT; US-PGPUB	2001/12/27 16:22
13	108	(functional adj2 unit$1) same (power near3 control$5)	USPAT; US-PGPUB	2001/12/27 16:22
16	9257	713/$.ccls.	USPAT; US-PGPUB	2001/12/27 16:22
22	5	((functional adj2 unit$1) same (power near3 control$5)) and ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))	USPAT; US-PGPUB	2001/12/27 16:23
19	22	713/$.ccls. and ((functional adj2 unit$1) same (power near3 control$5))	USPAT; US-PGPUB	2001/12/27 16:28
25	11332	(insert$3 or add$3) with (program$3 or (instruction adj stream$1))	EPO; JPO; DERWENT; IBM TDB	2001/12/27 16:46
30	136977	power near3 control$5	EPO; JPO; DERWENT; IBM TDB	2001/12/27 16:47
35	4412	functional adj2 unit$1	EPO; JPO; DERWENT; IBM TDB	2001/12/27 16:47
40	0	((insert$3 or add$3) with (program$3 or (instruction adj stream$1))) same (power near3 control$5) same (functional adj2 unit$1)	EPO; JPO; DERWENT; IBM TDB	2001/12/27 16:47

US-CL-CURRENT: **713/300**

US-PAT-NO: 6167330
DOCUMENT-IDENTIFIER: US 6167330 A
TITLE: Dynamic power management of systems
DATE-ISSUED: December 26, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Linderman; Mark H.	Rome	NY	N/A	N/A

US-CL-CURRENT: 700/295,**713/300**

ABSTRACT:
A method and system for power management of components within a system by introducing low-level instructions, such as NOPS, delay loops, and sleep modes,
into the instruction sequences within logical components of the system, thereby
allowing the system to maintain desirable power dissipation over a given time interval. Through employment of a control mechanism, a system can interrupt itself periodically to determine if the power dissipation must be limited and to what extent. A system can determine if and by how much it must limit its power by polling external components. The method may be implemented by a controller that intelligently manages power dissipation of components through selective manipulation of computer operations by selected components. Controll
of power dissipation for the selected components is intelligently based on overall system performance requirements. Furthermore, a plurality of sensors can measure power dissipation of a plurality of components in the system and cause the controller to selectively manipulate those components that require power management. In a proactive approach, power dissipation for the plurality
of managed components can be controlled based on known power characteristics for the selected components without necessarily monitoring the power dissipation of the system through sensors. In a reactive approach, a plurality
of sensors that measure power dissipation in the system can cause the controller to selectively manipulate components requiring power management. The system can employ a combination of proactive and reactive approaches to power management.
9 Claims, 7 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

DEPR:
The **insertion** of NOPs in the microprocessor is typically performed by the compiler for compiled code or in some instances by the **programmer** in assembly code. If the desired power dissipation is known at compile time, and the compiler for the system can approximate the power dissipation of a processor based upon the instructions it is executing, then the compiler may use this method of **controlling average power** by periodically stalling the processor to reduce the average power dissipation.

CCXR:
713/300

US-CL-CURRENT: 713/324

US-PAT-NO: 6128745
DOCUMENT-IDENTIFIER: US 6128745 A
TITLE: Power management inactivity monitoring using software threads
DATE-ISSUED: October 3, 2000
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Anderson; Eric	Sunnyvale	CA	N/A	N/A
Christopher	Los Gatos	CA	N/A	N/A
Farhi; Henri Hayim				

US-CL-CURRENT: 713/323,713/324
ABSTRACT:

A method for managing power in an electronic system having a plurality of input/output devices, each of the input/output devices having a full power-on state and at least one power reduction state and each being controlled by an associated device driver, the method comprising the steps of: initializing a power management logic separate from the device drivers to receive at least one
time-out value for each of the device drivers to be subject to power management; assigning a different timer in the power management logic to a different one of the device drivers to be subject to power management, the timers being disposed external of the device drivers; initializing each of a plurality of the assigned timers to individual predetermined value set in accordance with the at least one time out value of the assigned device driver for that timer; changing the individual predetermined value held in each of the
timers at a predetermined interval; monitoring a plurality of the timers and determining when the predetermined value in one of the timers indicates that the time-out value for the assigned device driver has elapsed, and sending a power reduction instruction to the assigned device driver; and resetting a given one of the timers to its individual predetermined value at any time when the device driver associated with the timer indicates a usage event of its associated device driver, and powering the associated device to a higher power level if it is not at full power-on.
25 Claims, 3 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 3

BSPR:
In yet a further aspect of the present invention, a **program** product is provided
comprising: at least one computer usable medium having computer readable **program** code means embodied therein to configure a computer to manage power, wherein operating system software controls the computer and is capable of controlling a plurality of input/output devices, each of the input/output devices having a full power-on state and at least one **power reduction state and**
each being controlled by an associated device driver, the computer readable **program** code means in the **program** product comprising: first computer readable code means designed to be **added** to each of the device drivers that is subject to power management, the first computer readable code means including a data structure for a name and at least one time-out value for a full power-on state and an API for power-up or power-lower for the device, the first computer readable code means functional to cause the computer to translate the API of the device to an API of a second computer readable code means; the second

computer readable code means designed to be **added** to each of the device drivers
that is subject to power management to facilitate communication between a power
management application (PMA) computer readable code means and the device associated with the device driver, the second computer readable code means having an API; third computer readable code means to cause the computer to initialize the second computer readable code means to create a thread for its device driver with a specific ID in order to support asynchronous communication
with the PMA computer readable code means. The PMA computer readable code means to cause the computer to provide a separate timer associated with each of
the device drivers, but external to the device drivers; wherein the second computer readable code means includes code to cause the computer to initialize the PMA computer readable code means to associate the full power-on time-out value for each of the devices with a different one of the timers; wherein the PMA computer readable code means includes code to cause the computer to monitor
each of the timers and if a given one of the timers associated with a given one
of the device drivers has a value indicative that its time-out value has been reached, then awakening the thread for the given device driver associated with that time-out value; wherein the third computer readable code means includes code to cause the computer to call the PMA computer readable code means for instructions upon awakening of the thread; wherein the PMA computer readable code means includes code to cause the computer to communicate to the second computer readable code means of the given device driver upon receipt of the call to lower at least one power level; and wherein the PMA computer readable code means includes code to cause the computer to reset a particular one of the
timers when the second computer readable code means of the device driver associated with the timer indicates a usage event for its associated device, and communicating to the device driver to power to a higher power if it is not at a full power-on state.

CCOR:
713/323

CCXR:
713/324

US-CL-CURRENT: 713/322

US-PAT-NO: 5825674
DOCUMENT-IDENTIFIER: US 5825674 A
TITLE: Power control for mobile electronics using no-operation instructions
DATE-ISSUED: October 20, 1998
INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Jackson; Robert T.	San Jose	CA	N/A	N/A

US-CL-CURRENT: 713/321,713/322

ABSTRACT:
A system for regulating power in a mobile electronics device uses "hint" NOP instructions having a reserved field of bits that generate control signals to affect an increase or decrease in power dissipation. The control signals raise or lower the operating potential provided by a power supply and also adjust the frequency of a clock signal in accordance with the information provided by the NOP instruction. Power is reduced for code sequences that could be executed more slowly, or the device is otherwise idle, without affecting the user's perception of overall system performance.
20 Claims, 8 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 5

BSPR:
The present invention overcomes the problems of the prior art by providing a system for regulating power in a mobile electronics device by the use of "hint" NOP instructions. The hint HOP instructions are **inserted** into a software **program**, such as an operating system or applications **program**, which is executed on a microprocessor. The NOP instruction includes an opcode field and a reserved field of bits that, when executed, provide information to a logic circuit which generates control signals that affect an increase or decrease in power for the mobile electronic device. The control signals raise or lower the operating potential provided by a power supply and also adjust the frequency of a clock signal in accordance with the information provided by the NOP instruction. In this way, the rate at which the processor (and the mobile electronic device) operates may be precisely **controlled by software such that power** is reduced for code sequences that can be executed more slowly without affecting the user's perception of system performance.

DEPR:
To better appreciate the operation of the system of FIG. 6, consider the following example. Assume that an operating system (i.e., DOS) is running on processor 310 and includes an idle loop. In accordance with the invention, a first special NOP instruction may be **inserted** by the compiler at the point in the **program** prior to execution of the DOS idle loop. For example, the NOP instruction may comprise a previously invalid instruction in the processor's instruction set architecture (ISA). The decode logic of the processor, however, may be modified such that the previously invalid instruction is now recognized as valid although it has no effect on the machine from an

architectural standpoint. Rather, the reserved bits of the instruction inform control logic to generate appropriate **control signals for the power** supply and clocking signal generator to effect an increase or decrease in power.

CCOR:
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CCXR:
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09/285,879

L Number	Hits	Search Text		Time stamp
1	9002	functional adj2 unit$1	USPAT; US-PGPUB	2001/12/27 16:46
4	135652	power near3 control$5	USPAT; US-PGPUB	2001/12/27 16:46
7	26606	(insert$3 or add$3) with (program$3 or (instruction adj stream$1))	USPAT; US-PGPUB	2001/12/27 16:46
10	0	(functional adj2 unit$1) same (power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))	USPAT; US-PGPUB	2001/12/27 16:22
13	108	(functional adj2 unit$1) same (power near3 control$5)	USPAT; US-PGPUB	2001/12/27 16:22
16	9257	713/$.ccls.	USPAT; US-PGPUB	2001/12/27 16:22
22	5	((functional adj2 unit$1) same (power near3 control$5)) and ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))	USPAT; US-PGPUB	2001/12/27 16:23
19	22	713/$.ccls. and ((functional adj2 unit$1) same (power near3 control$5))	USPAT; US-PGPUB	2001/12/27 16:28
25	11332	(insert$3 or add$3) with (program$3 or (instruction adj stream$1))	EPO; JPO; DERWENT; IBM TDB	2001/12/27 16:46
30	136977	power near3 control$5	EPO; JPO; DERWENT; IBM TDB	2001/12/27 16:47
35	4412	functional adj2 unit$1	EPO; JPO; DERWENT; IBM TDB	2001/12/27 16:47
40	0	((insert$3 or add$3) with (program$3 or (instruction adj stream$1))) same (power near3 control$5) same (functional adj2 unit$1)	EPO; JPO; DERWENT; IBM TDB	2001/12/27 16:47
45	140	(power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))	USPAT; US-PGPUB	2001/12/27 17:01
48	0	((power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))) and ((functional adj2 unit$1) same (power near3 control$5))	USPAT; US-PGPUB	2001/12/27 17:02
51	12	((power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1)))) and 713/$.ccls.	USPAT; US-PGPUB	2001/12/27 17:06
54	202782	driver$1	USPAT; US-PGPUB	2001/12/27 17:06
57	10	driver$1 same ((power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1))))	USPAT; US-PGPUB	2001/12/27 17:10
60	1	(driver$1 same ((power near3 control$5) same ((insert$3 or add$3) with (program$3 or (instruction adj stream$1))))) and 713/$.ccls.	USPAT; US-PGPUB	2001/12/27 17:10